



## **Modified Sidewall Design of QFN Package**

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### **Authors' contributions**

*This work was carried out in collaboration between both the authors. Both authors read, reviewed, and approved the final manuscript.*

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### **ABSTRACT**

The paper offers an improvement for leadframe devices to mitigate the occurrence of package chipping rejection during package mechanical singulation. The discussion provides a specialized design of mold chase for mold encapsulation process, and an augmented mechanical cutting technique of package singulation. Furthermore, insights are shared to apprehend the manufacturability of the improved design and process during assembly manufacturing specifically on the critical process steps of mold encapsulation and package singulation.

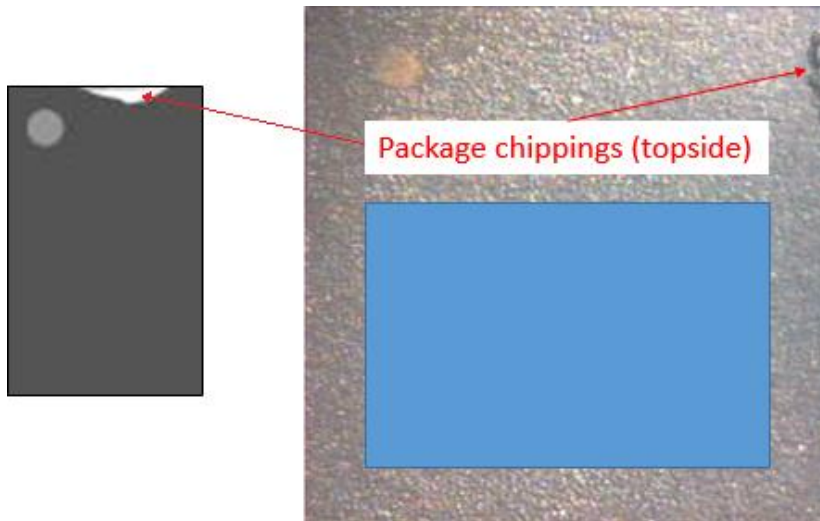
*Keywords: Leadframe; sidewall design; process improvement; QFN; package chipping.*

### **1. INTRODUCTION**

Leadframe device particularly quad-flat no-lead (QFN) package is manufactured from series of assembly processes, starting from die preparation or pre-assembly to package singulation and packaging. A QFN device is one

of the several packaging techniques under surface mount technology (SMT) wherein the silicon die is mounted on leadframe pad through die attach glue or tape [1-3]. The advantage of this architecture from other form of integrated circuit (IC) designs is its good thermal performance due to exposed thermal pads and

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**Fig. 1. Topside chipping of encapsulated package**

lower package stand-off, reduced lead inductance, smaller package dimension and thin profile [2-5]. The defect and rejection are closely monitored during these individual process steps, in order to produce a robust and quality device. Nevertheless, there are occurrences of defect escapee that could result to device malfunction and eventual external customer complaint.

Mold crack is one major reject during package singulation process, with the defect originating from large topside and sidewall package chippings of the package as shown in Fig. 1. Package chippings are the results of abrasion from the mechanical blade during cutting into individual units [6-8]. Many known approaches to minimize the chippings are available namely blade evaluation and selection, parameter optimization, and leadframe design resolution. However, these actions cannot fully eliminate the manifestation of the defect.

## 2. LITERATURE REVIEW AND DESIGN SOLUTION

A complete process flow for a standard QFN package starting from pre-assembly to back-end assembly until test and finish and packing is given in Fig. 2. Note that assembly and test process flow vary with the product and the technology [4-5,9].

A typical QFN design depicted in Fig. 3 is consist of an active silicon die bonded to a leadframe pad with the bond pads connected to the leads

through the bondwires (or simply wires) and is carefully governed by assembly design rules [2,7,10-11]. The unit is encapsulated by a mold compound material covering and protecting the internal devices. The standard package singulation process is through mechanical sawing, creating straight outline and abrasion mark on the sidewall part.

An improved design is shown in Fig. 4 with its cross-sectional representation. The indented sidewall is the modification and improvement on the design to mitigate the contact of mechanical blade during cutting. Chippings caused by abrasion can be significantly minimized with this leadframe design improvement.

A specialized molding process and the augmented mold chase design is highlighted in Fig. 5. The dimension and size of the specialized design for mold chase would depend on the package size requirement of the device.

The cutting method for the modified package design is demonstrated in Fig. 6, where the distance of the mechanical and indented sidewall depends on the package singulation cutting capability. The width of the mechanical blade is also considered for the device pitching.

Wire bonding diagram and process optimization should be considered carefully, conforming to the assembly design rules. With this, the wires should maintain acceptable clearance between the modified sidewall and the wire as emphasized in Fig. 7.

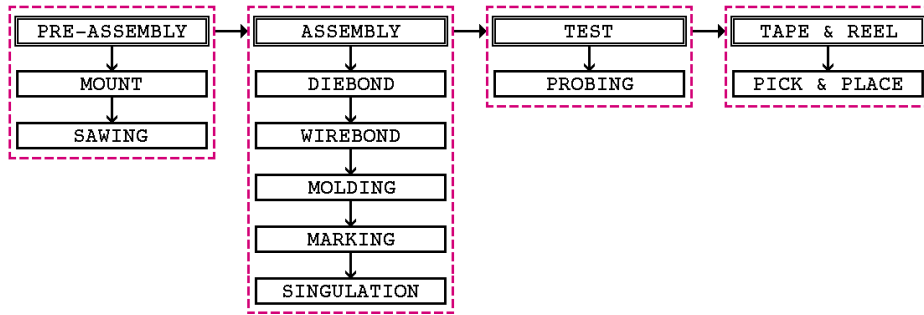


Fig. 2. Complete process flow

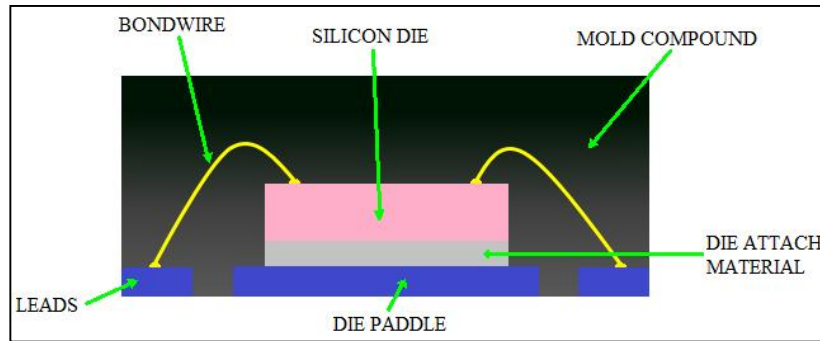


Fig. 3. QFN package cross-section representation

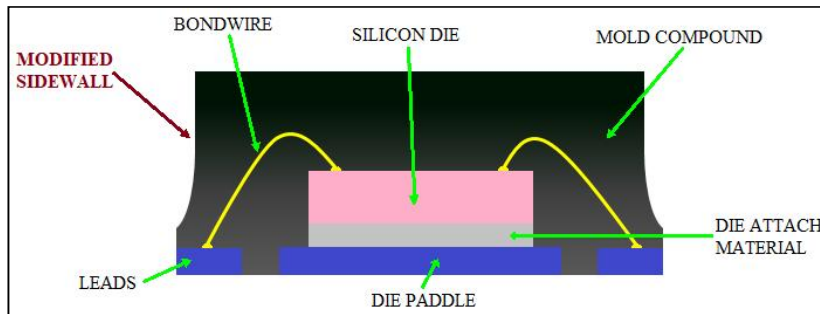


Fig. 4. Modified QFN leadframe design

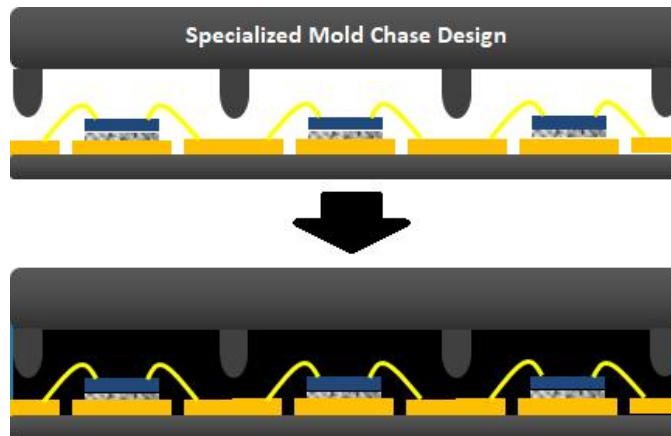


Fig. 5. Augmented mold chase design

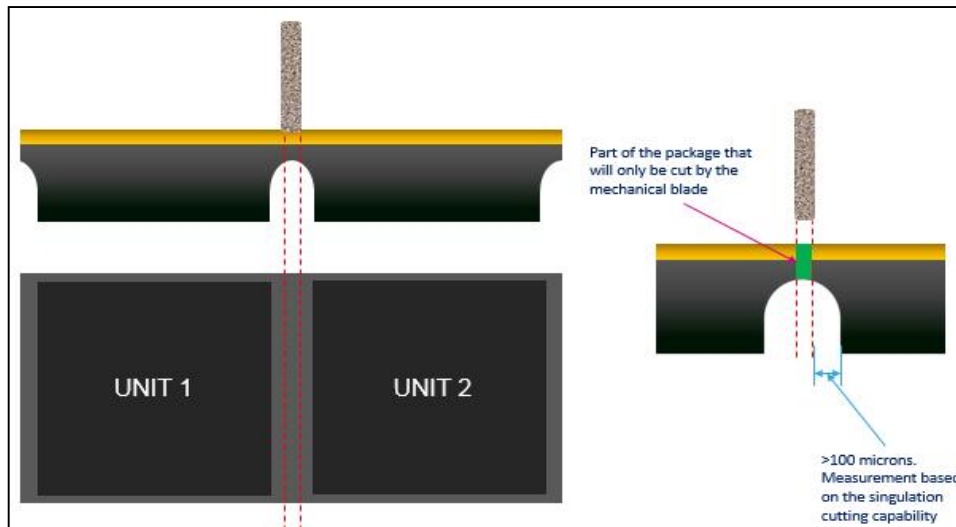


Fig. 6. Conventional package singulation using mechanical blade

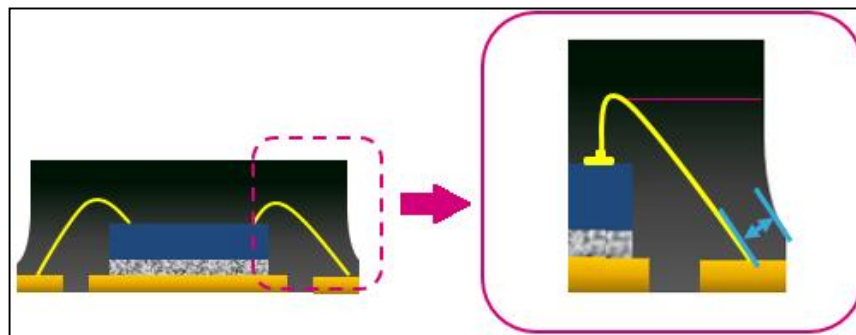


Fig. 7. Bonding diagram

One advantage of the improved design as compared to typical QFN design is that it helps prevent package chippings that could impact the quality of the devices. Moreover, mold delamination and mold crack are mitigated by the application of the modified and improved design. Lastly, cost reduction is also evident especially on blade life extension.

### 3. CONCLUSION AND RECOMMENDATIONS

Providing the improved and augmented design of QFN leadframe eliminates the occurrence of package chippings together with related defects such as mold delamination and mold crack. The modified design impacts the manufacturability through cost reduction initiative due to potential blade life extension.

Discussions shared in [8,12-13] are helpful to mitigate defects related to assembly process. Furthermore, it is worth noting that the assembly

manufacturing should observe proper electrostatic discharge (ESD) checks and controls. Learnings presented in [14] are very helpful to ensure proper and effective ESD-related controls.

### DISCLAIMER

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### COMPETING INTERESTS

Authors have declared that no competing interests exist.

### REFERENCES

1. Geng H. Semiconductor manufacturing handbook. 1<sup>st</sup> Ed., McGraw-Hill Education, USA; 2005.
2. STMicroelectronics. Procurement and quality general specification for metallic leadframe. rev. 8.0; 2019.
3. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; 2007.
4. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
5. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
6. Sumagpang A, Gomez FR. Specialized singulation punch design for package chip-out elimination. Journal of Engineering Research and Reports. 2019;5(2):1-7.
7. STMicroelectronics. Molding design rules specification for BGA packages. rev. 1.0; 2009.
8. Rodriguez R, Gomez FR. Incorporating package grinding process for QFN thin device manufacturing. Journal of Engineering Research and Reports. 2019;9(2):1-6.
9. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
10. STMicroelectronics. Assembly and EWS design rules for wire bond Interconnect dice. rev. 53.0; 2018.
11. STMicroelectronics. Advanced EWS and assembly design rules specification. rev. 34.0; 2018.
12. Bacquian BC, Gomez FR. A study of vacuum efficiency for silicon on insulator wafers. Journal of Engineering Research and Reports. 2019;6(1):1-6.
13. Sumagpang A, Gomez FR. A methodical approach in critical processes optimization of new scalable package semiconductor device for ESD applications. Asian Journal of Engineering and Technology. 2018; 6(6):78-87.
14. Gomez FR, Mangaoang T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr lead-frame devices. Journal of Electrical Engineering, David Publishing Co. 2018; 6(4):238-243.

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