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Modeling of Leadframe Strip Warpage after Die Attach Cure Process

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Author's contribution

The author performed the strip warpage modeling in this study and also read and reviewed the final manuscript.

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Short Research Article

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ABSTRACT

In the leadframe package assembly process, silicon die is attached to the leadframe using a die attach adhesive material and the bonded strip is then cured. However, excessive strip warpage after the die attach cure process is a challenging problem that also affects the succeeding assembly processes. In this study, strip warpage modeling was done using a finite element analysis (FEA) technique to understand the warpage mechanism after die attach cure and find options to reduce strip warpage. The effect of changing the leadframe thickness, die thickness, and the leadframe design in terms of the number of strip panels or changing the connecting bar was analyzed. Modeling demonstrated that lead frame contracts faster than the silicon die resulting in the "frowning" warpage that agrees with the actual observation. It was also shown that increasing the die thickness by 25% results in 27% warpage reduction. Results also showed that increasing the number of panels or maps in a strip could significantly reduce the strip warpage. Improving the panel-to-panel isolation using stress relief cuts is also another option to reduce warpage after die attach cure.

Keywords: Strip warpage; leadframe strip; die attach cure; warpage modeling.

1. INTRODUCTION

The semiconductor package is composed of different materials. When the package components are assembled, strip warpage commonly occurs due to the mismatch in the coefficient of thermal expansion (CTE) of each package component. Excessive strip warpage

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isa challenging problem in the semiconductor package assembly. One example of such problem is shown in Fig. 1 where there is an excessive warpage of the leadframe strip after the die attach cure process.

When strip warpage is high after die attach cure process, the strip could be crumpled or damaged during the succeeding processes. Difficulty in wire bonding could also be encountered resulting in non-stick on lead (NSOL) or non-stick on pad (NSOP) problems. It also poses a challenge to strip handling during the whole package assembly. The strip may get stuck during the loading of the strip to assembly machine equipment loaders.

Many studies on strip warpage [1-5] are dealing with warpage problem in a molded package. They include warpage analysis considering the impact of mold filling and curing steps, optimum combination of material properties, and the cure shrinkage of the mold compound. Wang et al. [6] studied strip warpage after molding process using bi-material strips (epoxy and copper). For laminate substrates, Lee et al. [7] suggested design optimization, mechanical/thermal treatment and low CTE material to reduce substrate warpage. It appears that there are more research activities done on strip warpage after the molding process than those assembly processes before molding like the die attach and wire bonding. Though it is very important to ensure that strip warpage is low for a molded package as it affects package strip singulation and the reliability of the finished semiconductor package, making sure the strip warpage is also low after die attach cure is equally important. The die-bonded strip would not reach the molding process if it has been damaged after die attach.

The current study would focus on analyzing the excessive strip warpage of a leadframe package after the die attach cure process to find some possible solutions to the problem. Different aspects of the package design were explored like the leadframe thickness, number of panels and die thickness to reduce strip warpage and avoid package assembly yield issues due to warpage-induced damage.

2. METHODOLOGY

2.1 Strip Warpage Modeling

To understand the warpage mechanism and be able to find options in achieving strip warpage reduction, strip warpage modeling was performed using finite element analysis (FEA). Finite element analysis has been used to do warpage modeling for molded strips in previous studies [1-4]. Some are using FEA techniques for improved prediction like the inclusion of cure shrinkage [3] or using the anisotropic viscoelastic shell modeling technique performed on the warpage simulations for a full microelectronic package with a multilayer PCB [8]. Other semiconductor package strip warpage studies use FEA in analyzing the effect of stress relief slots [9], mold compound fillers and die thickness [10], and the combination of mold cap thickness, substrate thickness and mold compound [11]. A simple and efficient image-based approach for simulating strip warpage as a function of temperature is also studied with FEA [12].

In the current study, no cure shrinkage or viscoelastic behavior was included to make the analysis faster for analyzing different options. The FEA model is shown in Fig. 2 with the die bonded to the leadframe strip. The stress free or zero warpage condition was set at 160^{o}C, the die attach cure temperature. Different lead frame thicknesses (0.125 mm and 0.20 mm) and die thicknesses (120 µm and 150 µm) were considered in the modeling. A design using solid leadframe connecting bar was also analyzed to check if it could help reduce the strip warpage. The FEA was done using ANSYS software. The model was using 3D solid elements and symmetry boundary conditions were applied. A temperature equal to 25^{o}C was applied as a thermal load to the FEA model to simulate the cool down process from die attach cure temperature to room temperature. Linear elastic material properties were considered for the leadframe, die attach adhesive and silicon die in the modeling.

In another set of modeling, different leadframe configurations in terms of panels or maps per strip (Fig. 3) were analyzed. The 2-map leadframe strip shown is where the excessive strip warpage problem was encountered. The other leadframe strip configurations (4-map and 5-map) are having approximately the same total strip length as the 2-map leadframe strip.

3. RESULTS AND DISCUSSION

Based on the modeling result for the 2-map leadframe strip shown in Fig. 4, strip panel warpage at room temperature is ~5.3 mm in “frowning” mode. This is the baseline warpage modeling result. Actual strip warpage also shows

the “frowning” mode, which confirms what is observed in the warpage simulation during cooling down from die attach cure temperature (160^{o}C) to room temperature (25° C).

As the die-bonded lead frame strip assembly cools down from the die attach cure temp, lead frame contracts faster than the silicon die that results in “frowning” warpage as shown in Fig. 5. This is due to the higher coefficient of thermal expansion (CTE) of the lead frame, which is approximately 6x higher as compared to the CTE of silicon die. This enables the lead frame to pull the strip assembly into a “frowning” warpage mode as shown. Warpage generally decreases as temperature difference or delta T decreases (i.e. between the cure temperature and room temperature).

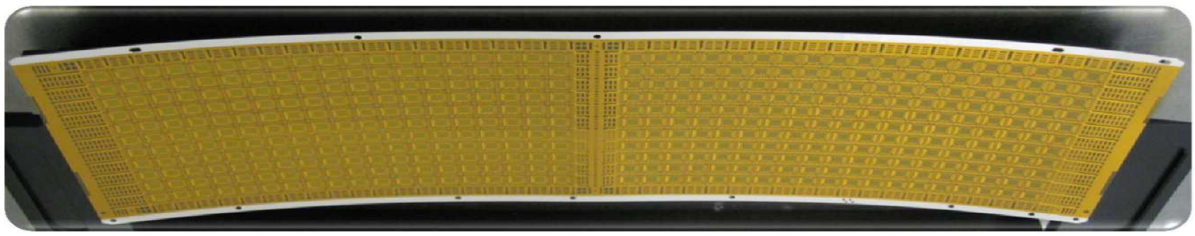

Fig. 1. Excessive leadframe strip warpage after die attach cure

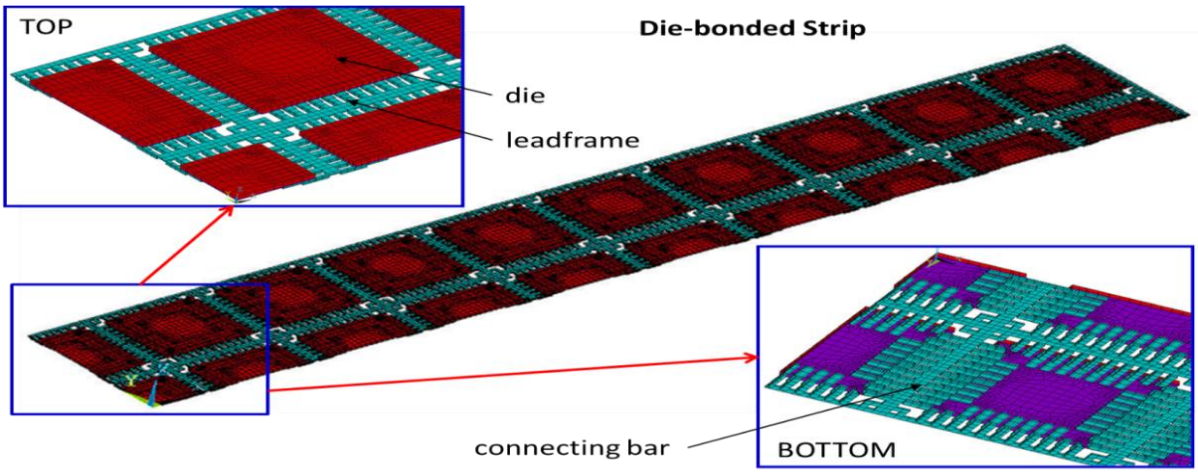

Fig. 2. FEA model of the leadframe strip with die bonded on it using die attach adhesive material

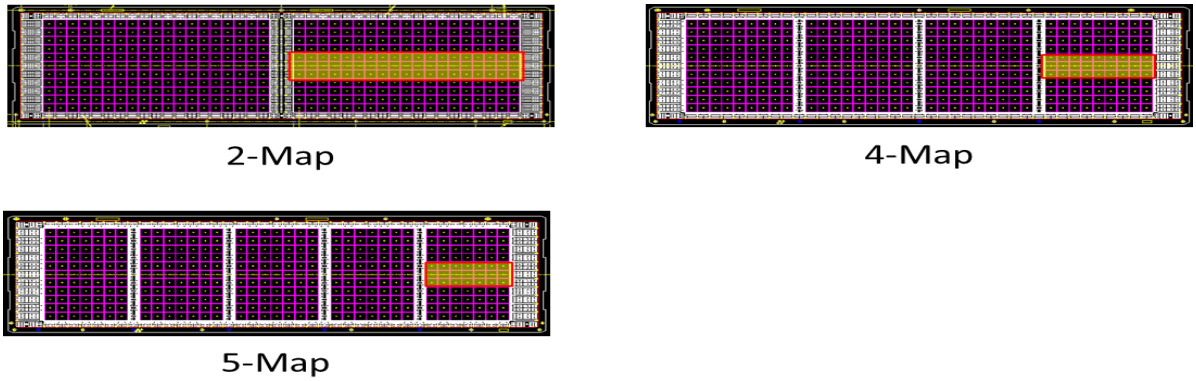

Fig. 3. Leadframe strips with different number of maps or panels

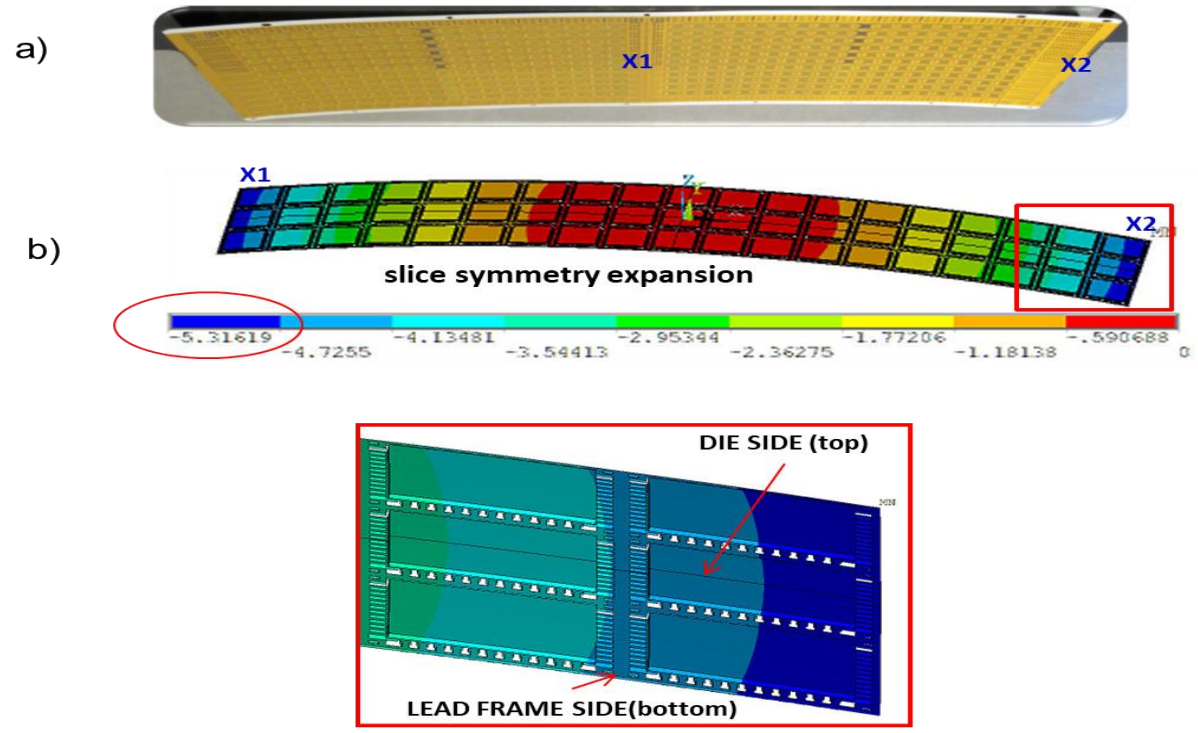

Fig. 4. Strip warpage results: a) actual leadframe strip, b) FEA simulation

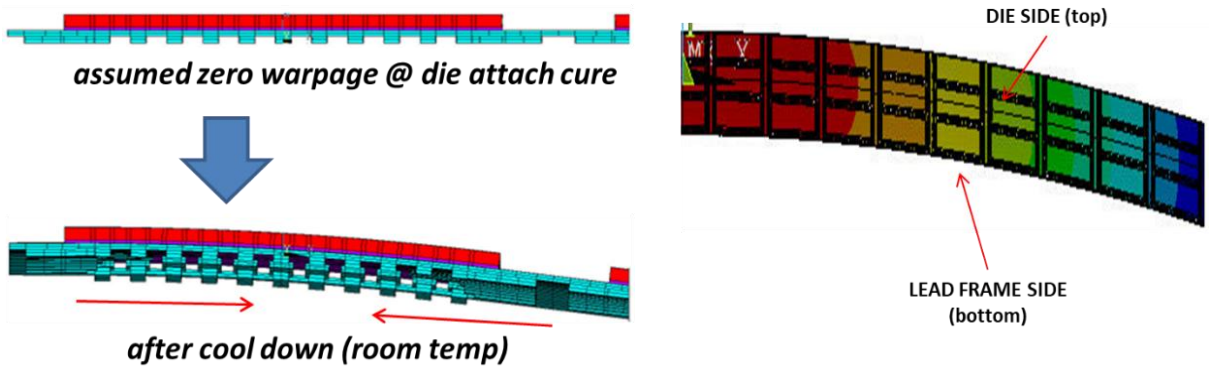

Fig. 5. Higher contraction of the leadframe causing "frowning" warpage after cool down process

The FEA modeling results as well as the normalized warpage values against the baseline are shown in Fig. 6. The normalized warpage was obtained by dividing the warpage result with that of the baseline warpage result. Increasing the leadframe thickness from 0.125 mm to 0.20 mm or using a solid connecting bar instead of a half-etched connecting bar shows no improvement in warpage reduction. However, increasing the die thickness from 120 µm to 150 µm provides significant decrease in warpage. The 25% increase in die thickness results in a 27% reduction in strip warpage. The increased stiffness with thicker die has shown to be beneficial in decreasing the strip warpage after die attach cure. This impact of die thickness on strip warpage after die attach cure turns out to be similar to the result of the related study [10] on a molded strip or when the package is already encapsulated.

Warpage simulation results shown in Fig. 7 are for each panel analyzed considering better isolation between panels. Results show that there is significant reduction in strip warpage from 5.3 mm to 1.3 mm when changing the leadframe configuration from 2-map to 4-map. The panel decoupling effect of better isolation is

provided by the strip relief cuts between panels as illustrated in Fig. 8. The results confirm the actual observation in package assembly manufacturing that the 4-map and 5-map leadframe strips are generally showing lower strip warpage. The issue of excessive strip warpage is mostly happening only on the 2-map leadframe strip.

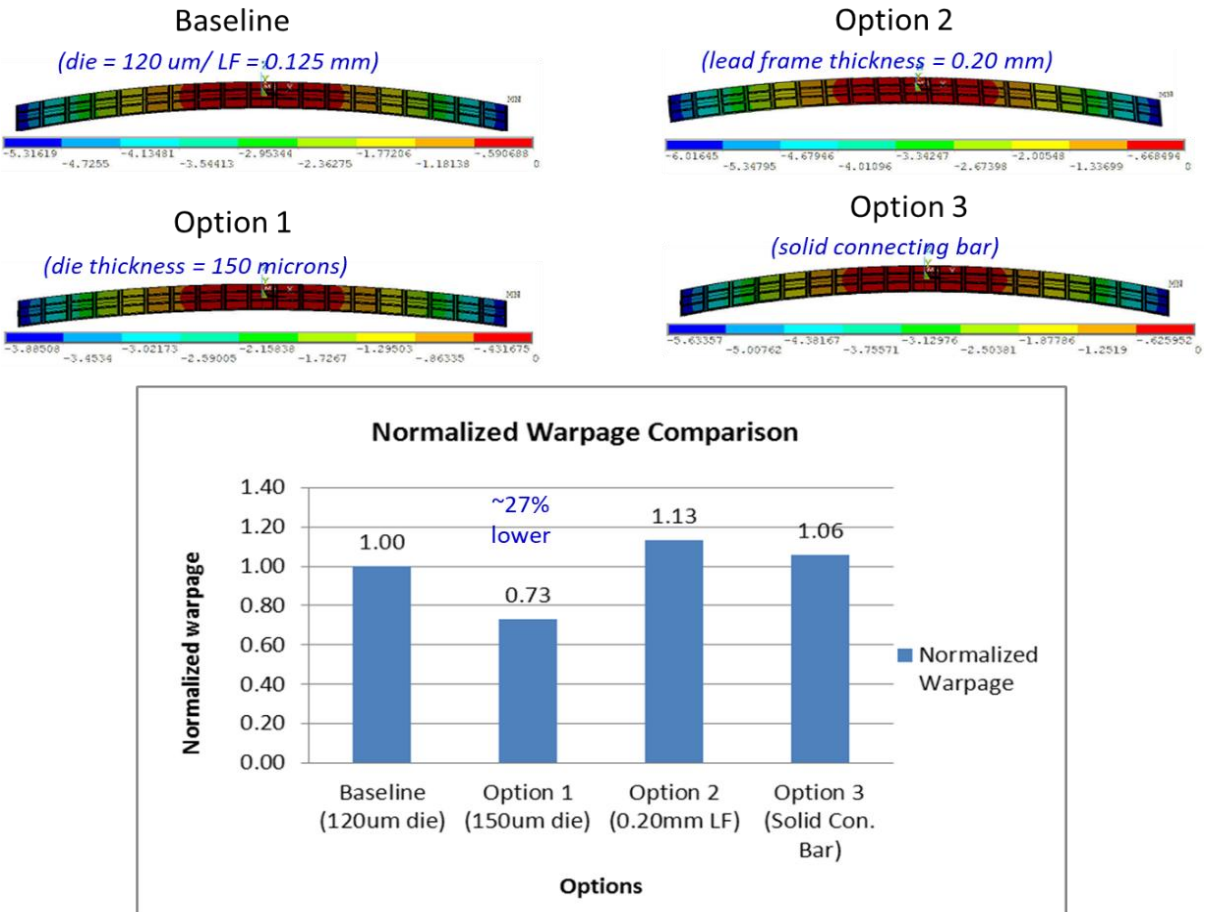

Fig. 6. Leadframe strip warpage comparison

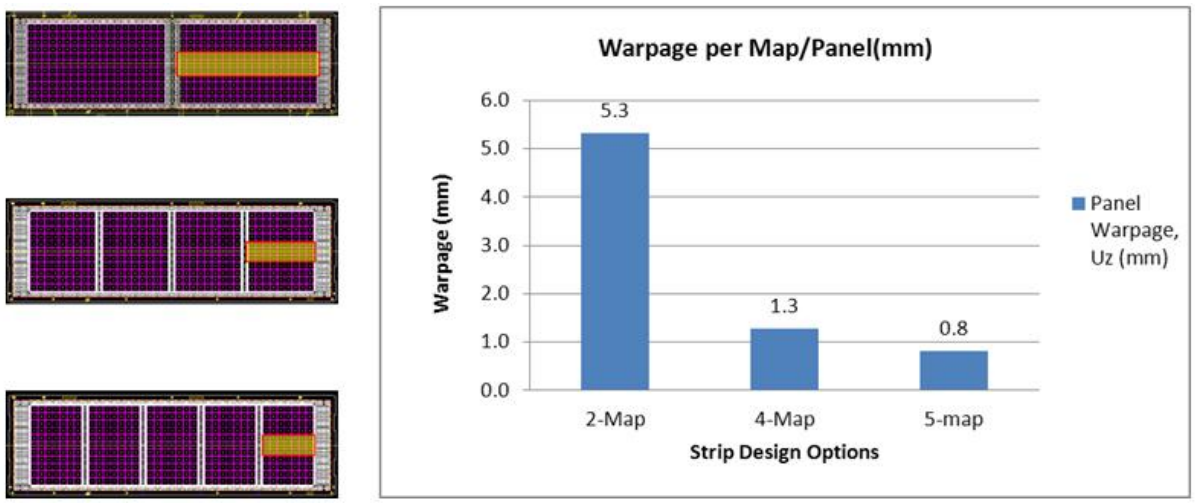

Fig. 7. Strip warpage results with higher number of panels or maps per strip

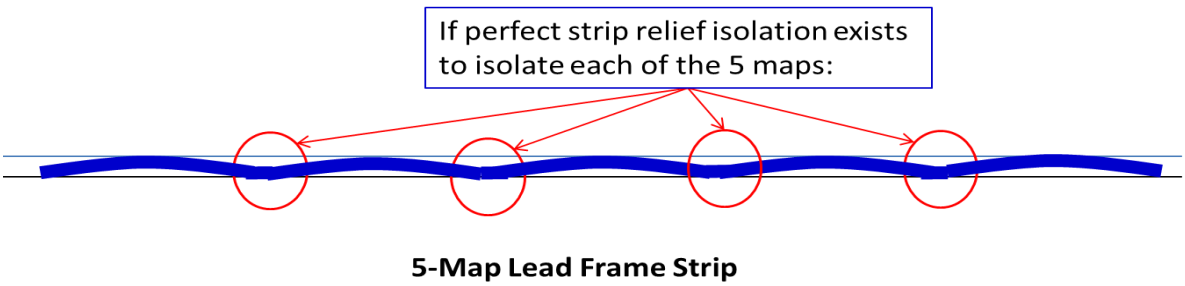

Fig. 8. Improving strip relief cuts to have better isolation and reduced warpage

4. CONCLUSION

Strip warpage modeling shows the same warpage mode as the actual die-bonded lead frame strip ("frowning") after cooling down from die attach cure process. This warpage mode is due to the higher CTE of the leadframe as compared to the silicon die. Strip warpage shows no reduction when lead frame thickness is increased from 0.125 mm to 0.20 mm (60% leadframe thickness increase) or when the half-etched connecting bar is converted to a solid connecting bar. However, warpage decreases by 27% when die thickness is increased from 120 µm to 150 µm (25% die thickness increase) in the current study. Warpage could also be lowered by increasing map-to-map or unit-to-unit isolation through improved strip relief cuts or increased number of maps or panels per strip. Based on modeling calculations, the new 4-map and the 5-map versions are predicted to have significantly lower warpage as also confirmed by leadframe strip warpage in actual package assembly manufacturing.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

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