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Understanding Package Crack Signatures in a Leadframe Semiconductor Package

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Author's contribution

The sole author designed, analysed, interpreted and prepared the manuscript.

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ABSTRACT

This paper presents the simulation approach used to understand package crack signatures of a leadframe package under different mechanical loading scenarios. Package crack is one of the common problems with semiconductor packages. A better understanding of the different crack signatures would help identify the root cause quickly and be able to find the correct solution. In this study, a high precision materials testing system was used to apply mechanical loading to the package simulating different scenarios that could produce the crack. Based on the testing results, cracks have distinct signatures depending on how the force is applied. With the different signatures identified, this approach makes it easy to find the root cause of the crack in actual applications or assembly processes and resolve the problem faster.

Keywords: Package crack; leadframe package; mechanical loading; crack signature; mechanical stress.

1. INTRODUCTION

In semiconductor packages, one of the issues commonly encountered during package manufacturing ang assembly and even in actual application is package crack. This is the case in which crack is found in the mold encapsulation that protects the whole integrated circuit (IC) die. When there is crack in the package encapsulation, moisture could easily damage the IC and prevents the device from functioning.

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Crack in the encapsulation could also propagate inwards resulting in a cracked IC die and eventually a non-functional device. Finding the true root cause is very important to eliminate the problem completely and prevent it from recurring.

For leadframe packages like Quad Flat No Lead (QFN), there are reliability challenges due to thermal, mechanical and chemical stresses as discussed in [1]. Package cracks/gaps can be caused by handling, electrical test operations, shipping and surface mount technology (SMT) printed circuit board (PCB) assembly [2]. Delamination can even result in package crack [3] and some problems can also be customer-attributable [4]. There are manuals or guides to avoid package problems. For instance, Epson [5] has a QFN package mount manual providing precautions when designing systems, handling or storing devices to minimize the chance of failure. There are other several studies [6-8] on reliability issues with packages under cyclic bending but focusing on the solder joint crack and not on package crack that is considered in the current study. Four point bending test of an overmolded leadframe sample was done by van Driel et al. [9] with the purpose of measuring the interface fracture toughness to address package interface delamination issues. Durability test on QFN packages under constant cyclic bending loadings was also analyzed using the approaches of signal processing technique involving comparison of strain response [10]. Three point bending technique of a QFN package was used for obtaining the flexural strength to understand the impact of gamma irradiation [11]. A related investigation on package cracking and delamination induced by clamping process was conducted using finite element software simulation and found that optimized clamping tool geometry and movement can reduce clamping induced stress and therefore can eliminate package cracking and delamination even if clamping a bent lead frame [12].

Fig. 1 shows an actual package crack problem from a customer complaint in a leadframe semiconductor package. Here, it is not clear where this could happen and what causes this kind of package crack. It could be that the package already has some small or hairline crack before it is mounted on the PCB. It could also be that this crack is induced during the mounting of the package. Without understanding the distinct package crack signatures, it would be very difficult and time consuming to find the real root cause. Then, there would be a possibility that the identified cause of the problem is not the correct one and the problem would only recur later.

In this study, a simulation was performed using a high precision mechanical testing equipment to understand the different package crack signatures under different mechanical loading conditions.

2. SIMULATING PACKAGE CRACK UNDER DIFFERENT MECHANICAL LOADING SCENARIOS

Using an Instron MicroTester that could be used to apply a certain amount of force, different loading conditions were simulated with the leadframe package and the cracks were inspected. Force was gradually increased from zero until a package crack was observed. The crosshead speed of Instron MicroTester was set at 0.10 mm/min to ensure any dynamic effects are eliminated as this study was focused on static loading conditions only. The package was tested when it was not yet mounted on the PCB. It was also tested as a package soldered to the PCB. The testing of the package not mounted on PCB would produce crack signatures that could be caused by the processes or steps prior to PCB mounting process. On the other hand, the testing of the board-mounted package would produce crack signatures during the PCB mounting process and the rest of the processes after soldering to the PCB. With this, it would be easier to pinpoint the real root cause of the specific package crack.

2.1 Materials Testing Equipment and Setup

The mechanical testing equipment used was an Instron MicroTester shown in Fig. 2. It has a load cell that measures the amount of force applied to the tested package in a 3-point bending setup as illustrated in Fig. 3. The leadframe package is supported at the bottom by 2 stationary anvils and force is applied from the top with the movable upper anvil.

2.2 Leadframe Package Tested

The package tested is shown in Fig. 4. The lead side is where the copper metal leadframe could be seen. The resin side is the opposite side where most of the resin used for package encapsulation is located. The IC die is attached to the exposed die pad using a die attach

material. The size of the leadframe package is 3 x 2 mm with a thickness of 0.55 mm.

2.3 Different Loading Scenarios

The different loading scenarios are shown in Fig. 5 for the leadframe package not mounted on PCB. The resulting crack signatures for each loading conditions were checked after applying a mechanical bending force to the package. For both Fig. 5a and Fig. 5b, the span or distance between anvil supports is 2.5 mm and for the setup shown in Fig. 5c, the distance is 1.75 mm.

On the other hand, the loading scenarios for package mounted on PCB are shown in Fig. 6. These are the loading setup conditions in which the leadframe package is already soldered to the PCB. The distance between anvil supports for Fig. 6a and Fig. 6c is 15 mm and 1.75 mm for Fig. 6b.

3. RESULTS AND DISCUSSION

For the first loading scenario in Fig. 5a, the package crack propagates from the top of the package (resin side) and is located at the package centerline as shown in Fig. 7. The breaking force or the force at which the package breaks in this loading condition starts at 28 N.

For the next loading scenario illustrated in Fig. 5b where force is applied to the resin side, the crack is now located at the die pad edge and it propagates from the bottom or the lead side to the top or the resin side (Fig. 8). The breaking force is a bit lower compared to the one in Fig. 7, where the resin side is facing downward. It appears that there is some weakening at the leadframe pad/mold intersection (leadframe side), which is subjected to tensile stress in this loading condition resulting in some reduction in force required to break the package.

With the offset loading of the package in Fig. 5c, the package crack is still located at the die pad edge. However, the crack propagation is now going in the opposite direction, that is from the resin side to the lead side as shown Fig. 9. The breaking force is higher in this loading condition compared to the two previous conditions since the distance between the two anvil supports is now shorter.

The resulting package crack for the first loading condition on a board-mounted package is shown in Fig. 10. The board or PCB is already cracked or damaged due to the bending force but the package is still intact. There is no damage to the soldered leadframe package and even to the solder joint. The force (>100 N) is already very high, but the package did not have any crack.

On the other hand, the crack is located at the die pad edge and propagates from the leadframe side of the package to the resin side (Fig. 11) for the loading condition illustrated in Fig. 6b. This happens because the exposed die pad is not soldered to the PCB and the force applied is causing the package to bend as the center of the package is not supported. It also needs much higher force (>100 N) to produce such crack in this loading condition since the location of the two anvil supports is close to the soldered lead. If the PCB with the soldered package is flipped such that the force is applied to the center of the package (resin side) and the PCB supported at the bottom by the two anvils, then the same package bending and crack signature would also be produced. The breaking force would then be much lower and close to the 25 N value obtained in Fig. 8 because the loading is now similar to Fig. 5b except that the package is soldered to the PCB.

For the offset loading on board-mounted package, the resulting crack is located at the lead or solder joint area as shown in Fig. 12. That area appears to be weaker than the resin area where the crack initiated in the case of the offset loading with the package not mounted on board (Fig. 9). The breaking force remains high in this loading condition.

With the crack signatures identified for the different mechanical loading scenarios simulated in a laboratory experimental setup, identifying the root cause would now be easier and faster. Going back to the package crack signature of the original problem reported (Fig. 1) and comparing with the distinct crack signatures from the simulated loading to the package, it can be observed that the package crack is very similar to the crack produced with the loading condition simulated in Fig. 6b with crack signature shown in Fig. 11. This means that the crack happens with the leadframe package soldered to the PCB and an external force is applied causing bending and then package crack because the exposed die pad is not soldered and supported against bending. The solution was then to solder the exposed die pad and control the amount of external force applied to the package mounted on PCB.

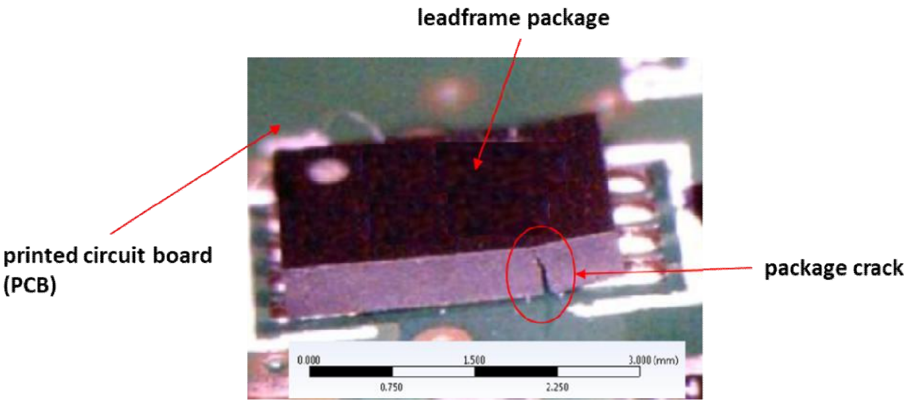

Fig. 1. Package crack in a leadframe package mounted on PCB

Fig. 2. Instron micro tester

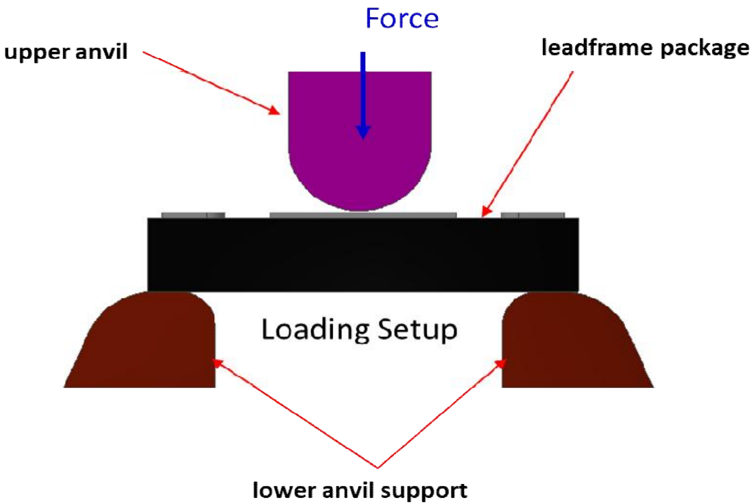

Fig. 3. Mechanical testing setup

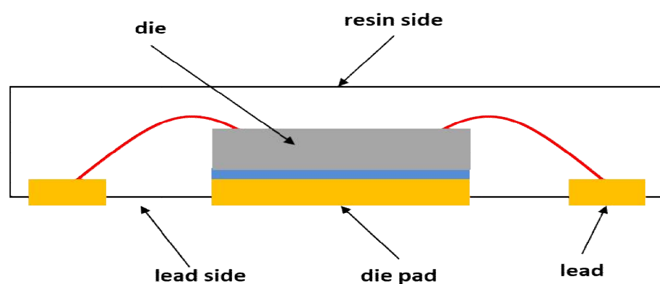

Fig. 4. Cross-section view of the leadframe package

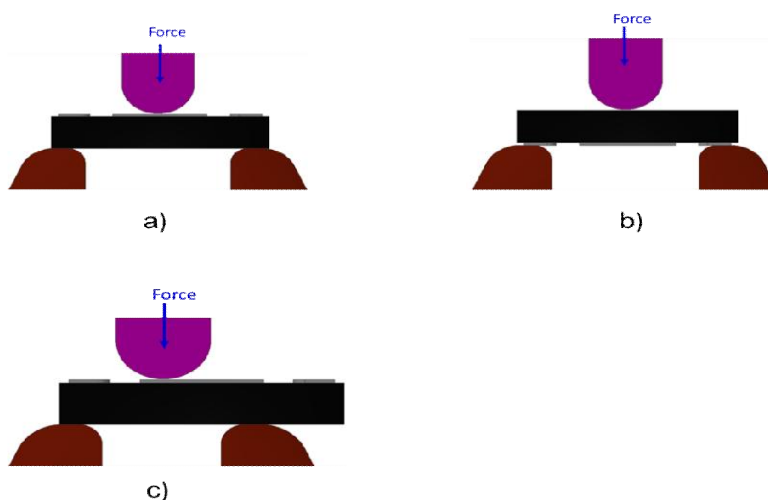

Fig. 5. Testing scenarios (package not mounted on PCB): a) centered with lead side oriented upward, b) centered with lead side oriented downward, c) offset

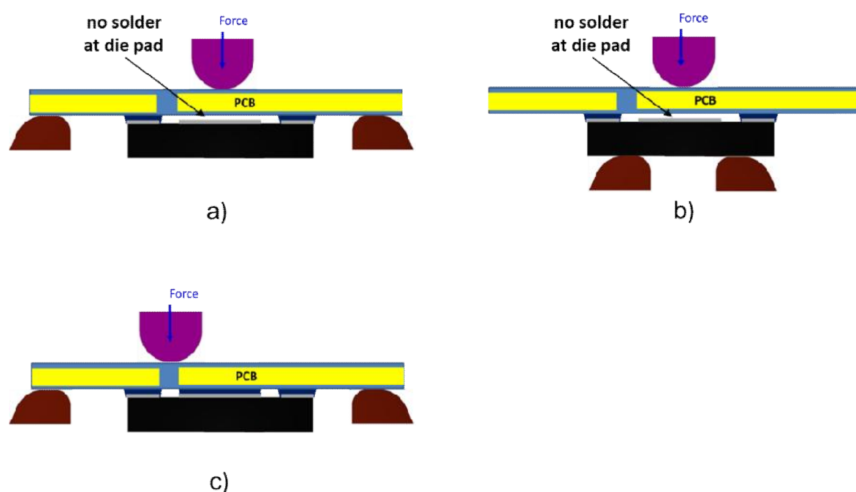

Fig. 6. Testing scenarios (package soldered on PCB: a) centered with no solder at die pad, b) centered but support is on the package, c) offset with support on PCB

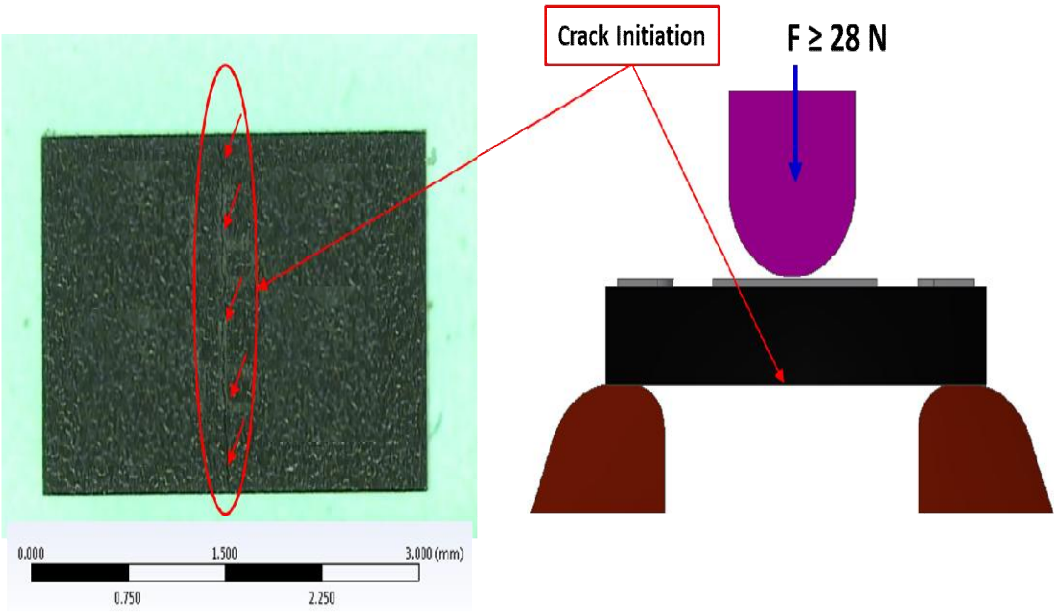

Fig. 7. Crack signatures for the tested package not mounted on PCB in Fig. 5a

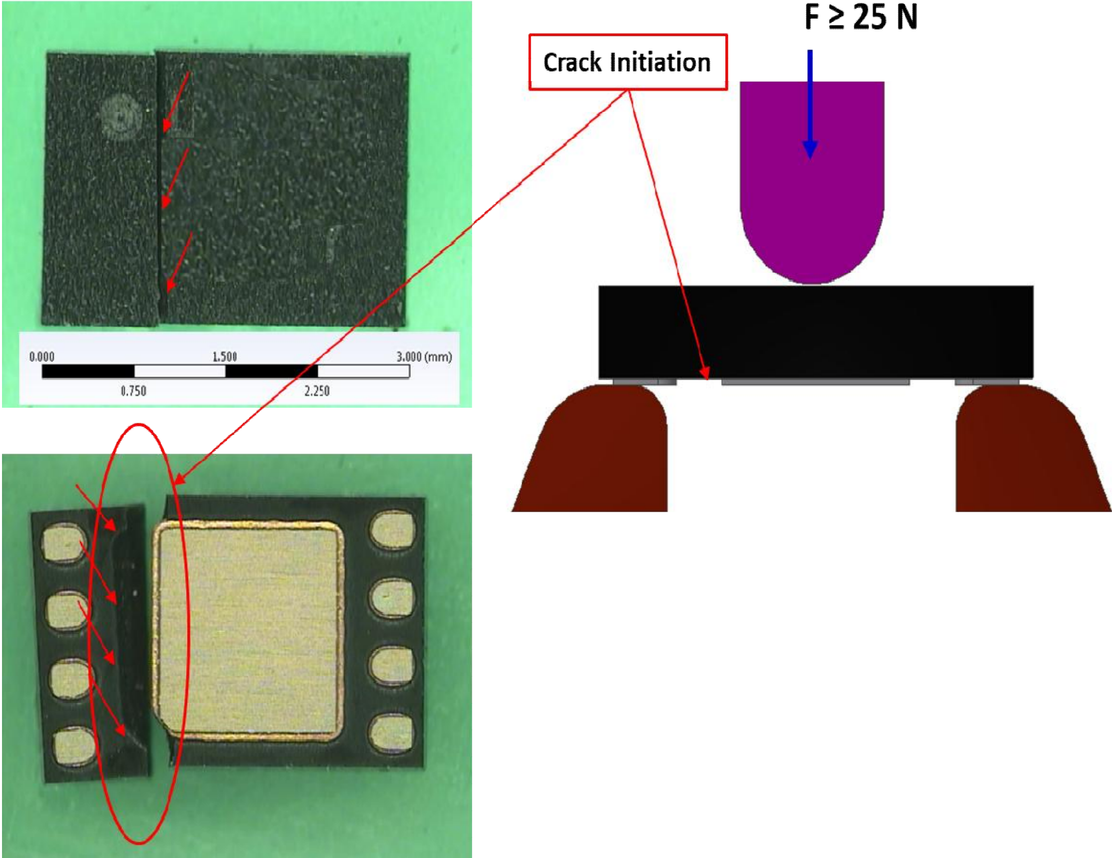

Fig. 8. Crack signatures for the tested package not mounted on PCB in Fig. 5b

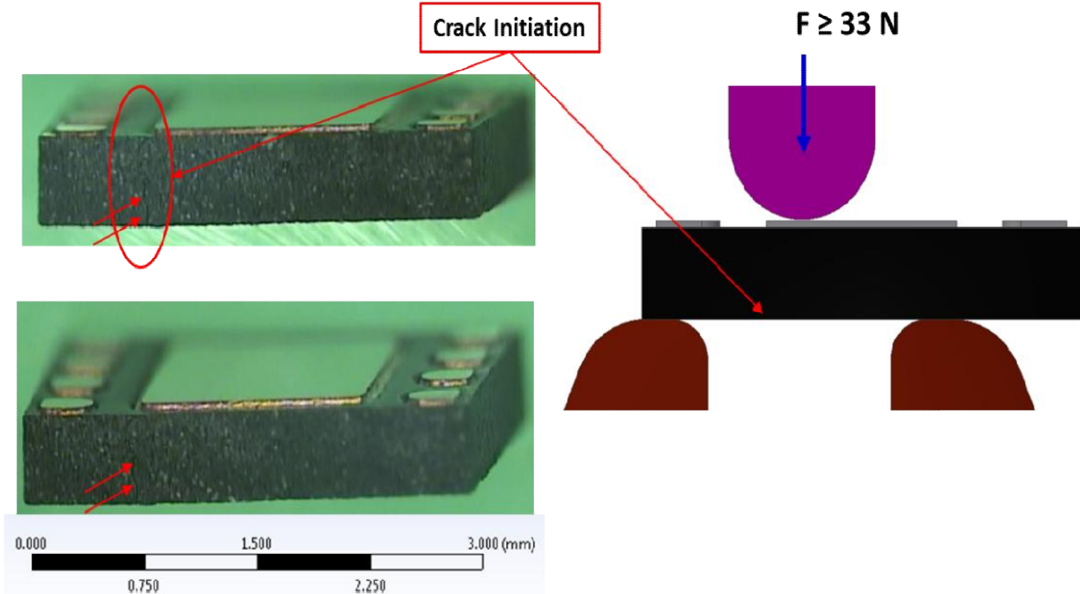

Fig. 9. Crack signatures for the tested package not mounted on PCB in Fig. 5c

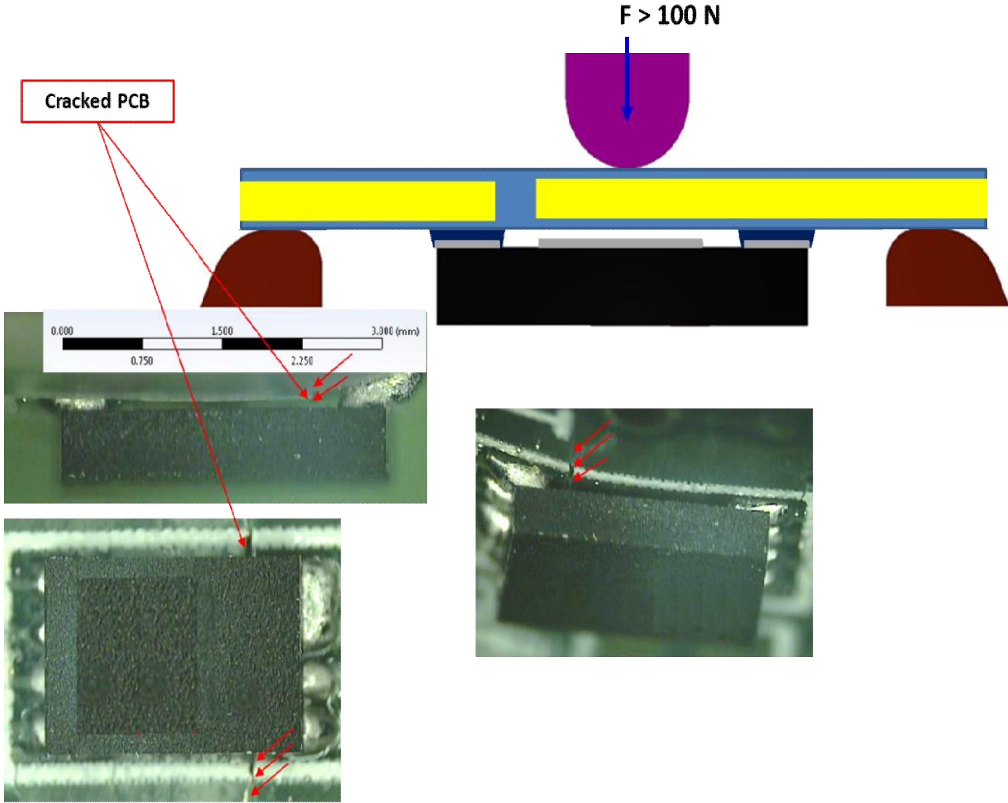

Fig. 10. Crack signatures for the tested package soldered on PCB in Fig. 6a

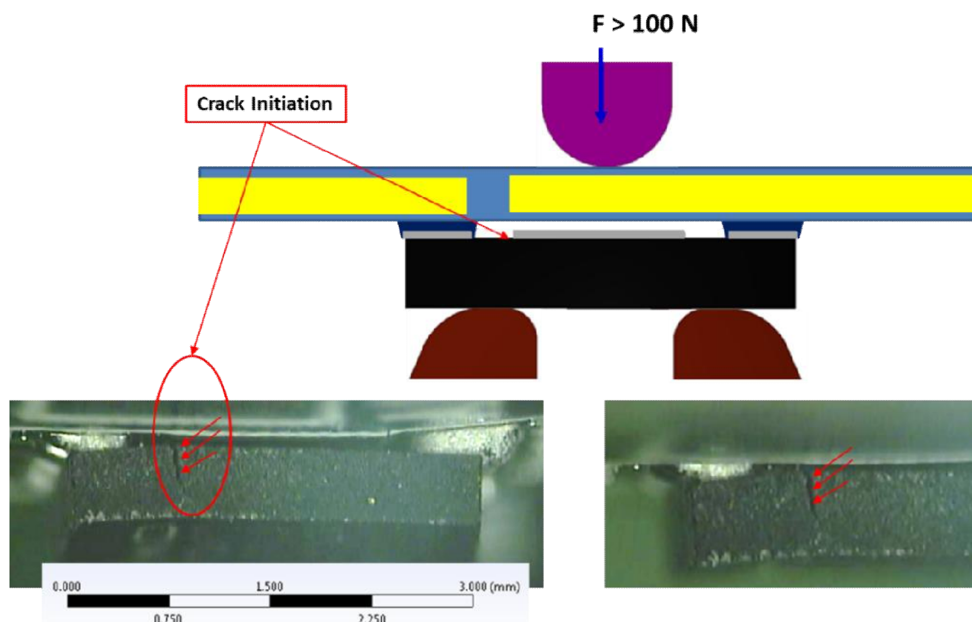

Fig. 11. Crack signatures for the tested package soldered on PCB in Fig. 6b

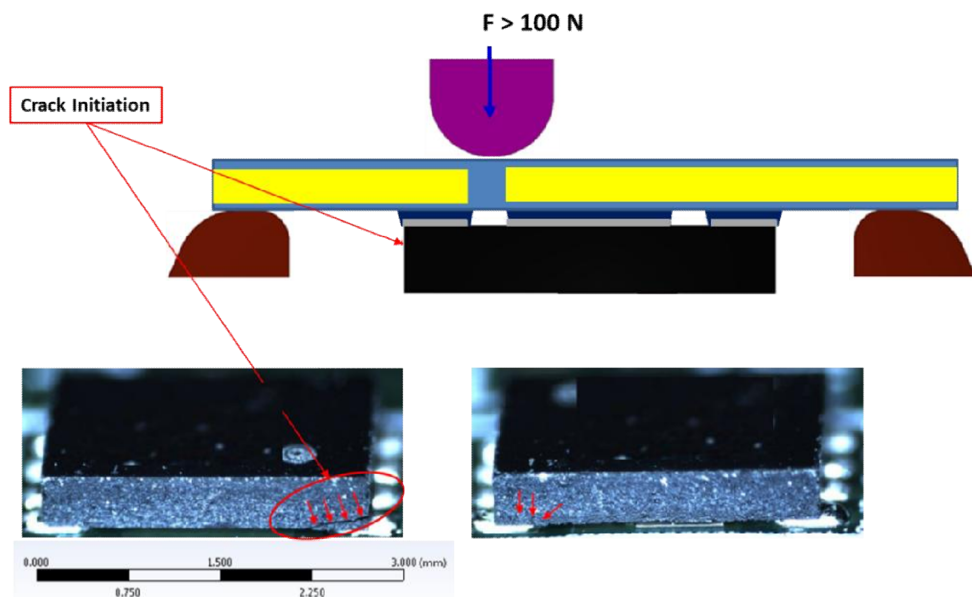

Fig. 12. Crack signatures for the tested package soldered on PCB in Fig. 6c

4. CONCLUSION

Using a high precision materials testing system in a laboratory experimental setup to apply mechanical loading to the package simulating different scenarios would be very useful in finding the root cause of a package crack problem. Package cracks, caused by external mechanical force, have distinct signatures depending on how the force is applied and how the package or PCB is supported. Therefore, knowing and understanding the different package crack signatures could help a lot in identifying the true root cause of the crack in actual applications or assembly processes and then a robust solution could be implemented. A recurring problem is

eliminated when the cause of the problem is correctly identified.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

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