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Warpage Mitigation through Diebond Process Improvement with Enhanced Leadframe Configuration

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed, and approved the final manuscript.

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ABSTRACT

This paper presents an improvement in the design of quad flat no-leads (QFN) leadframe material to reduce the amount of unit rejection due to excessive leadframe warpage observed after die attach curing (DAC) process. The enhanced leadframe design includes modification through increasing the number of unit panels from 2 maps structure into 4-panel configuration to integrate mechanical relief for coefficient thermal expansion (CTE) mismatch between different material composition present inside the device. The implementation of this design in the assembly of QFN successfully reduced the amount of leadframe warpage into manufacturable level with positive impact in production output and assembly yield.

Keywords: Quad flat no-leads (QFN); warpage; leadframe; coefficient of thermal expansion (CTE); die attach process; diebond process.

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1. INTRODUCTION

Die attach process is one of the preliminary process in integrated circuit assembly responsible for the picking and bonding process of silicon die from a wafer tape to a carrier. Conventional bonding structure includes a single integrated device diebonded on a single thermal pad, then connected to designated input/output (I/O) leads. Development in the semiconductor manufacturing enables bonding configuration of two or more silicon dies bonded in a single thermal pad, eventually to cater more I/Os in a small or limited package footprint.

In processing advance die bonding configuration, the assembly flow in Fig. 1 requires die attach cure (DAC) process after die attach or diebond. It is worth noting that assembly and test process flow varies with the product and the technology [1-5]. The mentioned process allows polymerization in the resin composition to make the glue hardened. This assembly setup is required for multiple die configuration to avoid disorienting the wet bonded units for the succeeding process steps.

The design of multiple die bonding configuration became critical due to the additional process steps of curing as compared to the conventional diebonding setup. One of the identified criticalities is the warping of the leadframe (or LF) strip shown in Fig. 2 that affects the assembly yield due to gross rejection of units.

2-map leadframe configuration, which is one example of leadframe used in semiconductor assembly particularly for quad-flat no-leads (QFN) device, is identified to induce worst warpage after subjected to heat during the DAC process. This eventually became an assembly barrier for advance bonding technology. In addition, it is pinpointed that it may also be the root-cause to decrease the reliability of the unit due to poor bonding condition found in the additional process step of die bonding and curing.

In this paper, a solution to overcome the worst warping for 2 maps configuration is presented through the application of 4-map leadframe design. Tangible benefits may be attained such as the manufacturability of multiple die bonding technology with acceptable assembly yields and positive results for reliability.

2. PROBLEM IDENTIFICATION

Warpage is known in thermomechanical analysis as the result of coefficient of thermal expansion (CTE) mismatch between the different material present in the architecture of the final product including the substrate, silicon die, molding compound. In addition, thickness and amount of material is also considered as contributor in the occurrence of the said problem. A thermomechanical analysis is often used to predict potential warping manifestation in a certain material combination. This tool was used

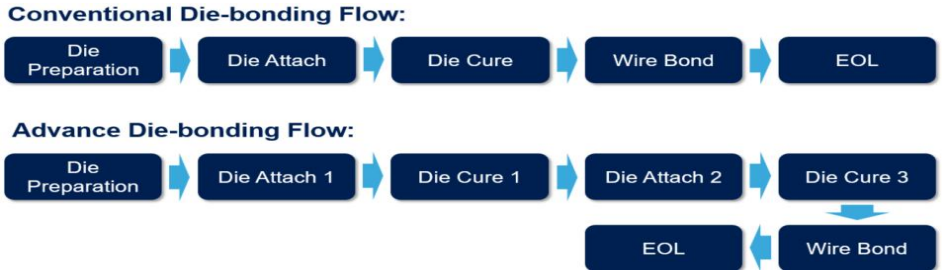

Fig. 1. Assembly flow

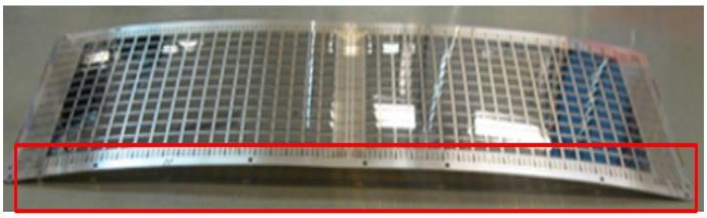

Fig. 2. Leadframe warpage after die attach process

to select the optimum material combination of a certain package design, to predict a design that has high probability to materialize. Eventhough warpage cannot be fully eliminated due to the different material composition and assembly design required to fabricate an integrated device, an alternative workaround is suggested to determine an acceptable warpage for leadframe that can still guarantee the manufacturability and productivity of the device.

The matrix in Table 1 is used to gather the acceptable warpage that can be processed by the machine, governed by assembly design rules and work instructions [4,6,7]. The success of the trial will be measured according to the occurrence of crumpled strips, misalignment, indexing errors which are the top assembly rejection related to warpage.

3. PROCESS DEVELOPMENT SOLUTION AND DISCUSSION OF RESULTS

The study of warpage is essential to determine the range of manufacturability factor of a device. Two trials presented in Fig. 3 and Table 2 were evaluated to determine the amount of acceptable warpage through incorporating two different LF configurations.

Table 1. Evaluation matrix

Trial	Configuration	Warpage	Crumpled strips	Mis-alignment	Indexing errors	Remarks
1	2-map LF					
2	4-map LF					

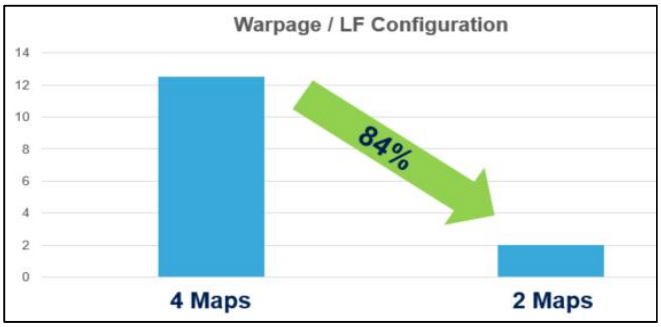

Fig. 3. Warpage comparison

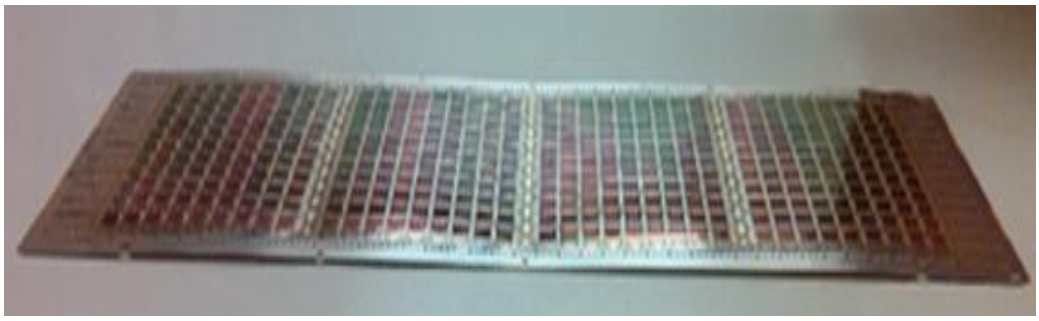

Fig. 4. Leadframe strip with 4-map configuration

Table 2. Evaluation results

Trial	Configuration	Warpage	Crumpled strips	Mis-alignment	Indexing errors	Remarks
1	2-map LF	< 15 mm	1	0	5	Fail
2	4-map LF	< 2 mm	0	0	0	Pass

The result from the evaluation shows that upon implementation of the new leadframe configuration, the warpage occurrence is reduced by 84% with actual warpage level of < 2 mm. The warpage in this case is accepted until < 2 mm since it does not induce manufacturing issue and machine errors. The improved solution in die attach process is done through augmenting the QFN leadframe configuration from 2 maps to 4 maps as depicted in Fig. 4. With the improved leadframe design, occurrence of warpage is significantly reduced. Robust process could be realized especially in the succeeding process stations with heat involved. The improved leadframe configuration could also improve the reliability of the package and could serve as an error-proofing design to control crumpled strips.

4. CONCLUSION AND RECOMMENDATIONS

The paper presented a process solution and improvement with the improved leadframe configuration, which significantly resolved the assembly reject occurrence of warped leadframe after die bonding process. The new leadframe configuration design offered a better warpage formation that cannot affect the succeeding process like, wirebond, molding, and sigulation. This new leadframe configuration provide good reliability test as well.

Continuous improvement is necessary to sustain high quality performance of assembly manufacturing. Discussions presented in [8-10] are helpful to mitigate defects related to assembly processes. Moreover, it is also important that the assembly manufacturing should observe proper electrostatic discharge (ESD) checks and controls. Learnings shared in [11] are helpful to comprehend proper and effective ESD-related controls.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; 2014.
2. Geng H. Semiconductor manufacturing handbook. 2nd Ed., McGraw-Hill Education, USA; 2017.
3. Hwang J. Solder paste in electronics packaging: Technology and applications in surface mount, hybrid circuits and components assembly. Ven Nostrand Reinhold, New York, USA; 1989.
4. STMicroelectronics. Package and process maturity management in back-end manufacturing. Rev. 7.0; 2018.
5. Coombs C, Holden H. Printed circuits handbook. 7th Ed., McGraw-Hill Education, USA; 2016.
6. STMicroelectronics. Work instruction for tape/DAF and glue diebond process. Rev. 66.0; 2018.
7. STMicroelectronics. Assembly and EWS design rules for wire bond interconnect dice. Rev. 54.0; 2019.
8. Bacquian BC, Gomez FR. A study of wafer backgrinding tape selection for SOI wafers. Journal of Engineering Research and Reports. 2019;6(2):1-6.
9. Huang HH, Wey J. Research on the high-speed pick and place device for die bonders. 8th IEEE International Conference on Control and Automation. 2010;2(2).
10. Rodriguez R, Gomez FR. Pick and place process optimization for thin semiconductor packages. Journal of Engineering Research and Reports. 2019;4(2):1-9.
11. Gomez FR, Mangaoang T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.

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