



# **A Comprehensive Study for Specialized Silicon-on-Insulator Wafers**

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### **Authors' contributions**

*This work was carried out in collaboration amongst the authors. Both authors read, reviewed and approved the final manuscript.*

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## **ABSTRACT**

The relentless advancement and trends on thinner packages have become the focus in the semiconductor manufacturing industry. The requirement of thinner packages also demands a thinner vertical structure of the semiconductor electronic design. As a major contributor on the vertical structure of the electronic package, die or wafer is also essential to go thinner. As the wafer becomes thinner, various problems may occur during transport and even the backgrinding process itself.

Wafer warpage is one of the main concerns during the wafer backgrinding process. Insufficient vacuum may cause non-planar wafer in contact with the chuck table that may result to poor grinding and broken wafer. Wafer backgrinding stress and backgrinding tape tension also contribute to the effect on wafer warpage. Challenges exist in processing different silicon wafer technology, particularly the silicon-on-insulator (SOI) technology. Evaluating the effect of backgrinding tape selection and vacuum efficiency to eliminate such warpage is presented in this paper.

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## 1. INTRODUCTION

Attaining the package requirements of a semiconductor electronic product would mean achieving a thinner die during the back-end process. The major process brick responsible for grinding the silicon die to its thickness is wafer backgrinding. As a major preliminary process at the back end, one of its sub-processes is the wafer preparation prior grinding wherein silicon wafer is been taped on the active layer to protect it from any contaminants and water penetration during the grinding process.

During backgrinding process, wafer is vacuumed on a chuck table to ensure wafer flatness. Wafer should be properly mounted to ensure or eliminate leakage that may cause flatness issue and will theoretically generate uneven grinding. However, original equipment manufacturers (OEM) have different designs of chuck tables in terms of porous area where vacuum is applied. One major factor for wafer warpage after grinding is the wafer backgrinding. The adhesion strength of the tape will induce the amount of wafer warpage and edge chipping of the grinded wafer. Ultimately, the paper focuses on the effect of different backgrinding tapes that can handle wafer warpage and discusses the importance of vacuum efficiency during the process.

### 1.1 Silicon-on-Insulator Wafer

Silicon-on-insulator (SOI) wafer technology uses a layered silicon-insulator-silicon substrate. With this technology, parasitic capacitance is reduced and thereby improving performance [1]. The

technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronics popularly referred to as extending Moore's Law [2]. SOI process has been developed intended for radio frequency (RF) applications [3]. The inclusion of enhanced sapphire substrate allows the complementary metal-oxide semiconductor (CMOS) node to have a high isolation, high linearity, and electrostatic discharge (ESD) tolerance. The glass passivation on the top layer in Fig. 1 creates a stepping effect on the edge of the wafer.

SOI wafers are measured prior wafer taping process and was observed to have the edge area 30 microns ( $\mu\text{m}$ ) thinner than the device, with warpage measurement in Fig. 2 of about 0.5 mm around the edge area [4].

### 1.2 Chuck Table Design

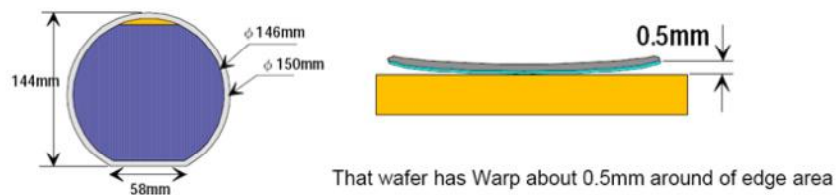
Chuck table ensures wafer flatness during wafer backgrinding process. Furthermore, wafer flatness is dependent on the amount of wafer clamp vacuum pressure and helps compensate wafer warpage during backgrinding process. The vacuum source pressure must be identical to wafer clamp vacuum, else, vacuum leakage would happen [4].

Chuck table varies between different wafers backgrinding OEM. Specifically, chuck table differs on the area where vacuum is applied. The table has a porous design where vacuum would be effectively distributed over the given area.



**Fig. 1. Wafer edge structure cross-sectional view**

[ Sample condition: design size & warp ]



That wafer has Warp about 0.5mm around of edge area

**Fig. 2. Wafer warpage after taping**

### 1.3 Wafer Backgrinding Tape

Wafer backgrinding tape is the main protection of the wafer on the stresses evident during mechanical grinding. Moreover, backgrinding tape helps eliminate water penetration, breakage or cushioning adsorption during grinding process, and maintains uniformity after grind, which have been verified by total thickness variation (TTV) [5,6]. Tape adhesion strength should be carefully evaluated to prevent wafer breakage and to check for adhesive contamination. The tapes are classified according to its adhesive material: conventional non-ultraviolet (non-UV) type and UV-curable type.

The two different types of backgrinding tape have been used to check if it helps adsorb the grinding stress and prevent wafer breakage during grinding and/or detaping process, given the inherent wafer warpage of the SOI wafers. Both tapes have almost the same tape thickness of 124 to 125 microns, but are different on the adhesive material used.

## 2. LITERATURE REVIEW

### 2.1 Wafer Warpage

As the semiconductor electronics device goes smaller and thinner, the trend of IC packaging also follows but becomes more complex. The requirement of thinner wafers is also being continuously developed. One major problem in the trend is the wafer warpage that would incur breakage during transport. Nevertheless, improvement is also done with acceptable process window of handling thin wafer. It is worth noting that subsequent assembly and test

process flow also adapt with the development and trend on wafer technology [7,8].

Vacuum efficiency acts as the major contributor of reducing or even eliminating wafer breakage during the automatic backgrinding. Two parts of the system that will require higher vacuum efficiency are the robot arm and chuck table. Low vacuum at robot arm will lead to errors during transport or worse, wafer breakage. However, low vacuum at the chuck table will cause inferior grinding.

### 2.2 Wafer Warpage Mechanism

A common wafer mechanism is a normal warpage [4,5] shown in Fig. 3. This is generally caused by the natural stress created by mechanical backgrinding. The proportional relationship of wafer warpage and mechanical stress states that when the final thickness decrease this probably caused by high mechanical stress that may lead to high wafer warpage.

### 2.3 Mechanical Stress after Wafer Backgrinding

Stresses incurred during encapsulation may crack the die and cause other stress-related failures. It is important to optimize the wafer strength to ensure reliability during both fabrication and packaging of wafers. However, grinding process inevitably results to flaws on its surface, which eventually weakens both the wafer and the individual dice sawn from it. These flaws may then spread into active regions and eventually results to die crack, with thermal or mechanical stress.

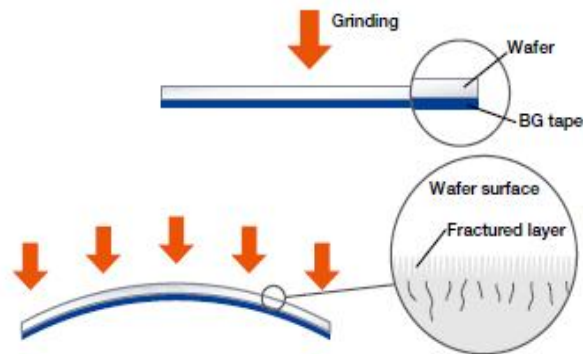


Fig. 3. Typical “frowning” warpage

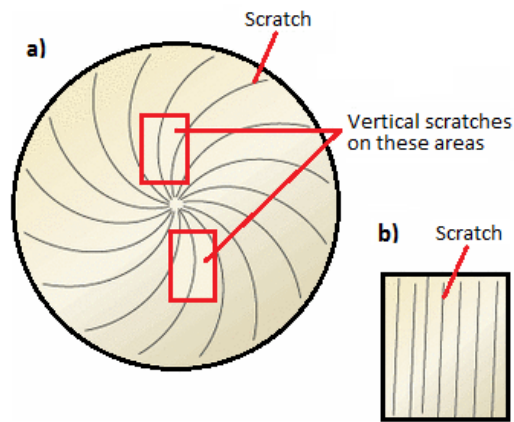
Source: Bacquian and Gomez [4]

The wafer exhibits a scratch pattern on the backside after backgrinding process as shown in Fig. 4. The scratch patterns and the depth of the scratches on the surface of the wafer are directly proportional to the size of the grit and the pressure exerted on the wafer during the grinding process. The depth of the scratches and the backside surface roughness of the semiconductor die has a direct correlation to the strength of the die, hence it is important that the finished backside surface of the wafer be as smooth as possible [6,9,10].

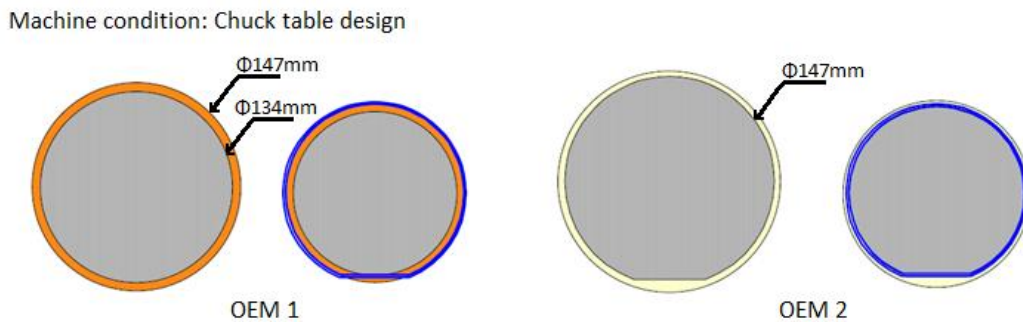
### 3. ACTUAL EVALUATION

#### 3.1 Machine Optimization

SOI wafers on a 6 inches diameter outline have been used to evaluate the capability of two OEMs. Wafer warpage was also noticeable prior loading to both evaluation machines. The two different OEMs in Fig. 5 have difference on the chuck table, wherein OEM 1 has a smaller porous area compared to OEM 2 by 13 microns. The porous area of OEM 2 is also observed to be on the same diameter as the OEM 1.



**Fig. 4. Vertical scratches after wafer backgrinding**  
Source: Bacquian and Gomez [4]



**Fig. 5. Chuck table design**

**Table 1. Backgrinding tape configuration**

| Specification      | Unit      | Conventional | UV Tape   |
|--------------------|-----------|--------------|-----------|
| Total thickness    | microns   | 125          | 120       |
| Adhesive thickness | microns   | 20           | 40        |
| Adhesion strength  | N / 25 mm | 2.84         | Before UV |
|                    |           |              | After UV  |
|                    |           |              | 0.1       |

### 3.2 Backgrinding Tape Selection

One major factor that could help minimize the wafer warpage is the backgrinding tape. Proper selection of the tape involves the study of the adhesion strength of the tape towards the wafer during wafer backgrinding thus inducing a much more wafer warpage after backgrinding. Two different backgrinding tapes in Table 1 have been evaluated to help reduce the wafer warpage prior and after wafer back grinding. Both tapes are on almost the same thickness, 125 and 120 microns, respectively. Conventional tape is observed to have lowered adhesion strength before UV compared to UV backgrinding tapes. However, UV types improves to 0.1 N / 25 mm after UV exposure that could possibly help lessen the stress of the backgrinding tape during the detaping issue thus reducing wafer warpage. Wafer warpage and wafer edge chipping will depend on the effectiveness of the wafer backgrinding tape.

## 4. RESULTS AND ANALYSIS

Two different chuck tables have different responses on the efficiency of the vacuum during wafer handling prior backgrinding. OEM 2 with the big diameter of the porous area on the chuck table with 147 mm cannot handle the step type passivation of the SOI wafer. Clamping error was encountered due to low vacuum efficiency of 80% on the OEM 2 chuck table. Full auto mode is also cannot be performed caused by low vacuum pressure that is not enough to handle the wafer before backgrinding.

OEM 1 with a smaller porous area exhibits a 95-100% vacuum efficiency. SOI wafer are properly seated on the chuck table therefore ensuring no leakage is encountered on between surface

contacts of the wafer. Full auto mode is also enabled and then preceded to auto backgrinding process. However, during the unloading of the finished wafer, vacuum errors occurred in Fig. 6 due to higher wafer warpage after backgrinding. There is a manifestation of vacuum leakage due to extreme wafer warpage. Afterwards, manual intervention is also cannot be performed due to vacuum leakage and that leads to manual unloading of the wafer on the robot arm.

Both backgrinding tapes in Fig. 7 induced wafer edge chippings and wafer warpage. The amount of wafer warpage for both tapes shows comparable level after backgrinding. Wafer edge chippings are observed being similar for both tapes. The readings of both tapes showed potential cause of wafer breakage. Both wafer backgrinding tapes have not been successful to be processed using the full auto mode due to its high warpage during the unloading. The robot arm vacuum is not enough to handle even the minimum warpage of 3.0 mm.

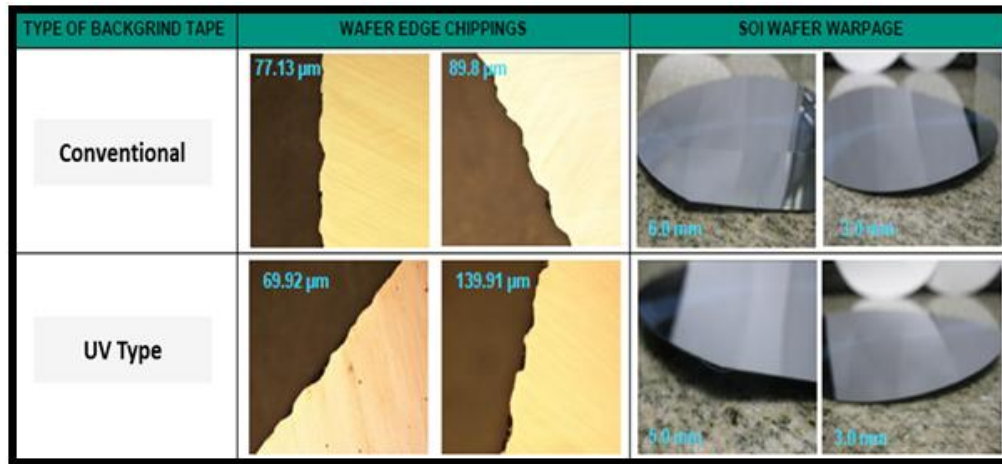
Back side image of the wafer in Fig. 8 shows uneven surface at the edge of the wafer, which can be considered a potential cause of broken wafer during transport process from one station to another at pre-assembly. Also, the occurrence of uneven surface at the back of the wafer also coincide with the step at the edge of the wafers.

Table 2 summarizes the risk level of the evaluated backgrinding tape configuration, having no significant effect across all critical wafer backgrinding responses, namely broken wafer, wafer edge chippings and warpage. Moreover, wafer surface structure has significant effect on the quality index of its wafer backgrinding manufacturability.

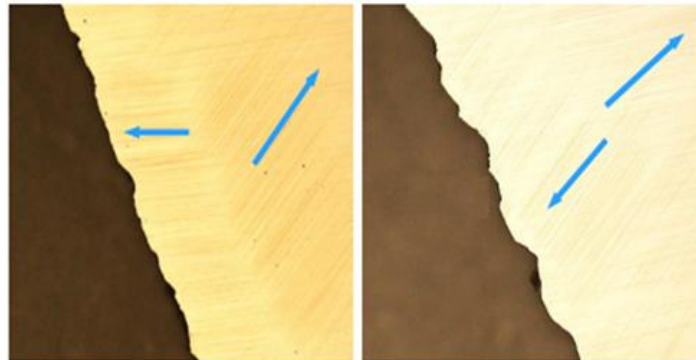


**Fig. 6. Vacuum error on the robot arm**

*Source: Bacquian and Gomez [4]*



**Fig. 7. Wafer edge chipping and warpage**  
 Source: Bacquian and Gomez [6]



**Fig. 8. Back side image of the wafer**  
 Source: Bacquian and Gomez [4]

**Table 2. Quality index**

| Backgrinding tape | Broken wafer | Wafer edge chippings | Wafer warpage | Risk level |
|-------------------|--------------|----------------------|---------------|------------|
| Conventional      | Medium       | High                 | Medium        | High       |
| UV Type           | Medium       | High                 | Medium        | High       |

Source: Bacquian and Gomez [6]

**5. CONCLUSION**

Chuck table design is important in handling special wafer surface design. Vacuum efficiency should be properly studied to ensure no leakage on the chuck table during the grinding process. However, the smaller porous size of the chuck table caused the uneven surface at the back side of the wafer due to no vacuum holding the overhang structure on the edge of the wafer.

Adhesion strength of the wafer backgrinding tape was negated by normal warpage phenomena on the wafer. The backgrinding tape, even on UV

type tapes, could not equalize the amount of mechanical stress on the wafer surface structure thus increasing the effect of wafer warpage towards the silicon wafer. Both tapes also could not negate the step type structure of the wafer thus creating wafer edge chippings and could be resulting wafer warpage if not fully controlled during handling.

For future works, it is recommended to use high vacuum efficient chuck table to properly handle incoming wafer warpage. It is to ensure good flattening on the chuck table and eliminate the possibility of inferior grinding. In addition, a

special process should be considered in making an outer circumference lip, where no grinding pressure is applied on the edge of the wafer during backgrinding. Discussion shared in [11-13] on critical processes such as wafer saw, are helpful to mitigate or eliminate defects associated with assembly manufacturing. Moreover, it is highly important that the processes ensure proper and acceptable ESD controls and checks. Implementations shared in [14] could be helpful to realize ESD-related controls.

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The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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## COMPETING INTERESTS

Authors have declared that no competing interests exist.

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